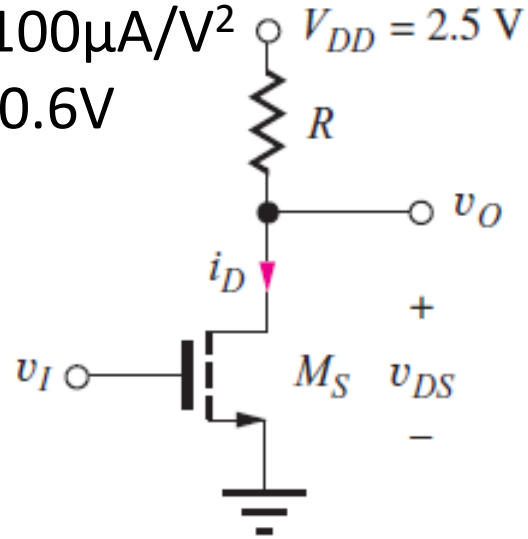
NMOS resistive load inverter

K_n'=100μA/V²
V_{TN}=0.6V



$v_I = v_{GS}, v_O = v_{DS}$

Design: Chose *R* and *W/L* of M_S

- A resistor load to "pull" the output up toward the power supply V_{DD}.
- Switch between two states:
  - Triode region: $v_I = V_H \Rightarrow v_O = V_L$
  - Cutoff region: $v_I = V_L \Rightarrow v_O = V_H$

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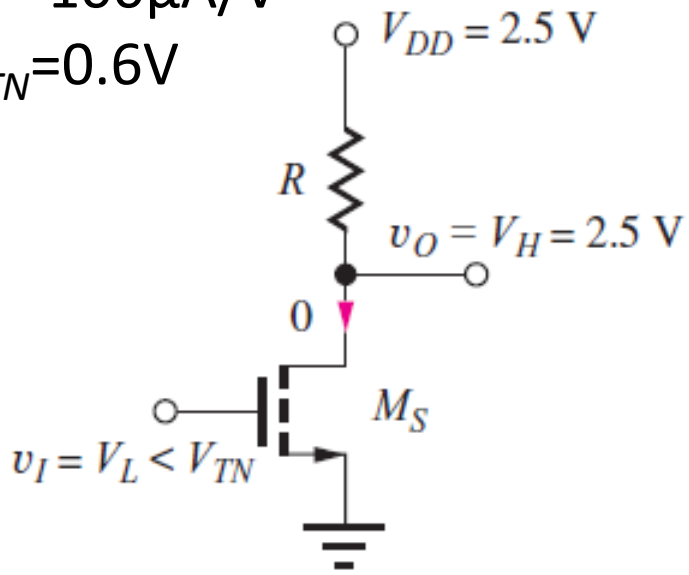


$v_I = V_L, v_O = V_H$

$v_I = V_L$, M_S cutoff

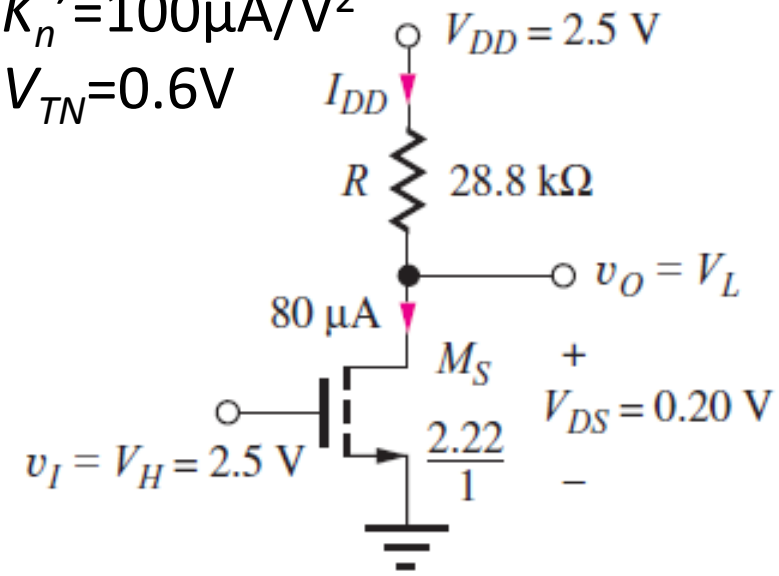
- $i_D = 0 \Rightarrow v_O = V_H = V_{DD}$
- V_H is set by power supply voltage V_{DD}.
- V_L should be less than V_{TN}, typically $V_L \sim 0.2$ V

Announcements

- HW #5 due today
- Exam 2 in class on Monday 5/19
  - MOSFETs
  - MOSFETs in circuits and NMOS Logic
  - HWs 4-6

Design of $\left(\frac{W}{L}\right)_S$ and R

K_n'=100μA/V^2
V_{TN}=0.6V



$v_I = V_H, v_O = V_L$

Current determined by permissible power dissipation of the NMOS, $\boldsymbol{P = V_{DD} I_{DD}}$

$v_I = V_H$, M_S triode

- Drain current (P=0.20 mW, V_{DD}=2.5V)

$$I_{DD} = \frac{P}{V_{DD}} = 80\ \mu\text{A}$$

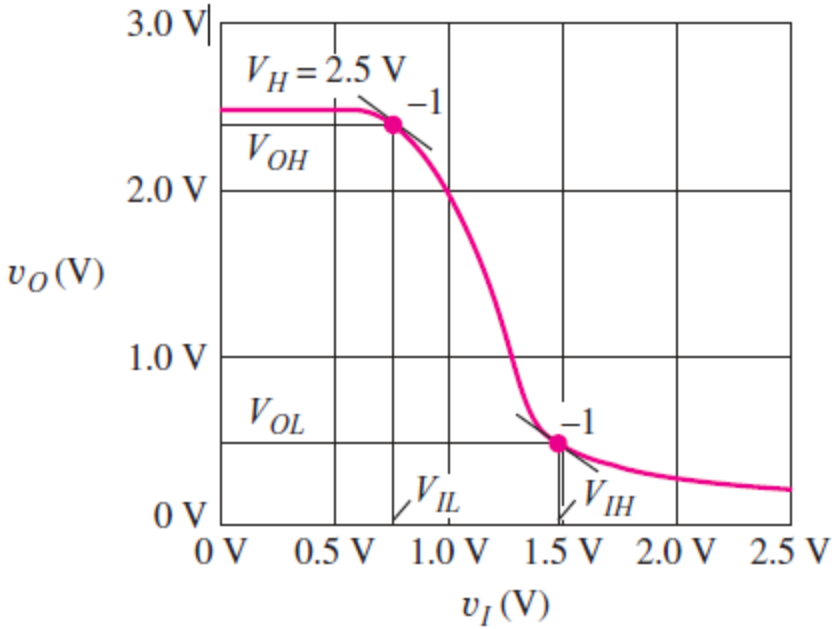
- Triode region equation:

$$i_D = K_n' \left(\frac{W}{L}\right)_S \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right) v_{DS}$$

- $v_{GS} = V_H = 2.5$ V, $v_{DS} = V_L = 0.2$ V
  $\Rightarrow \left(\frac{W}{L}\right)_S = \frac{2.22}{1}$
- Load resistor:

$$R = \frac{V_{DD} - V_L}{i_D} = 28.8\ \text{k}\Omega$$

Noise Margin Analysis

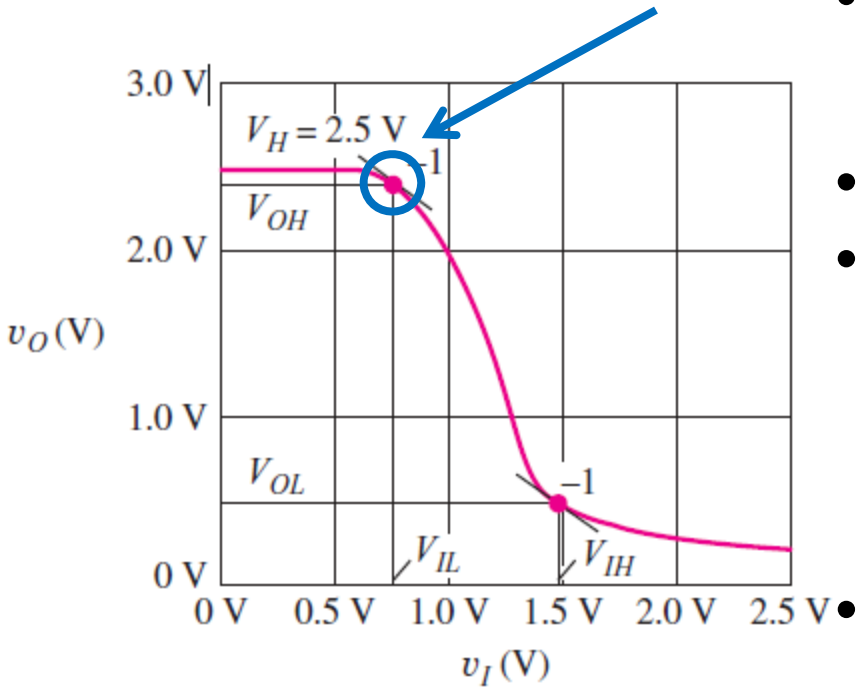


Procedure:

- Find relation between v_O and v_I
- Calculate (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}) by $\frac{dv_O}{dv_I} = -1$
- Calculate noise margin by

$$\mathrm{NM}_L = V_{IL} - V_{OL}$$
$$\mathrm{NM}_H = V_{OH} - V_{IH}$$

Calculate (V_{IL}, V_{OH})



- v_{GS} small and v_{DS} large, saturation:

$$i_D = \frac{K_n}{2}(v_I - V_{TN})^2 \quad ①$$

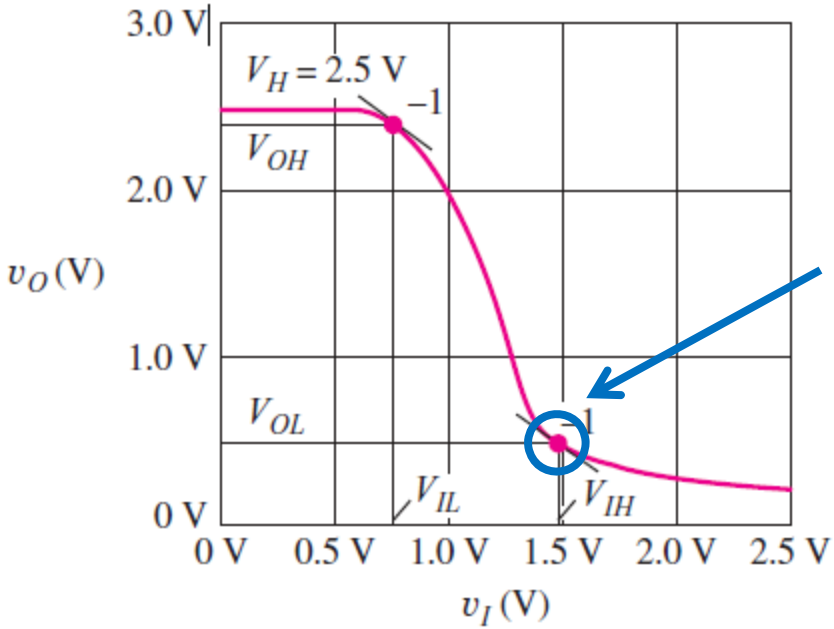
- Load Line: $v_O = V_{DD} - i_D R$ ②
- Combine ①②:

$$v_O = V_{DD} - \frac{K_n R}{2}(v_I - V_{TN})^2$$

$$\Rightarrow \frac{dv_O}{dv_I} = -K_n R(v_I - V_{TN})$$

- Setting $\frac{dv_O}{dv_I} = -1$, we get
  - $V_{IL} = V_{TN} + \frac{1}{K_n R}$
  - $V_{OH} = V_{DD} - \frac{1}{2K_n R}$

Calculate (V_{IH}, V_{OL})



You can write v_O in terms of v_I and solve for $\frac{dv_O}{dv_I} = -1$, but that's tedious!

- v_{GS} large and v_{DS} small, triode:

$$i_D = K_n\left(v_I - V_{TN} - \frac{v_O}{2}\right)v_O \quad ①$$

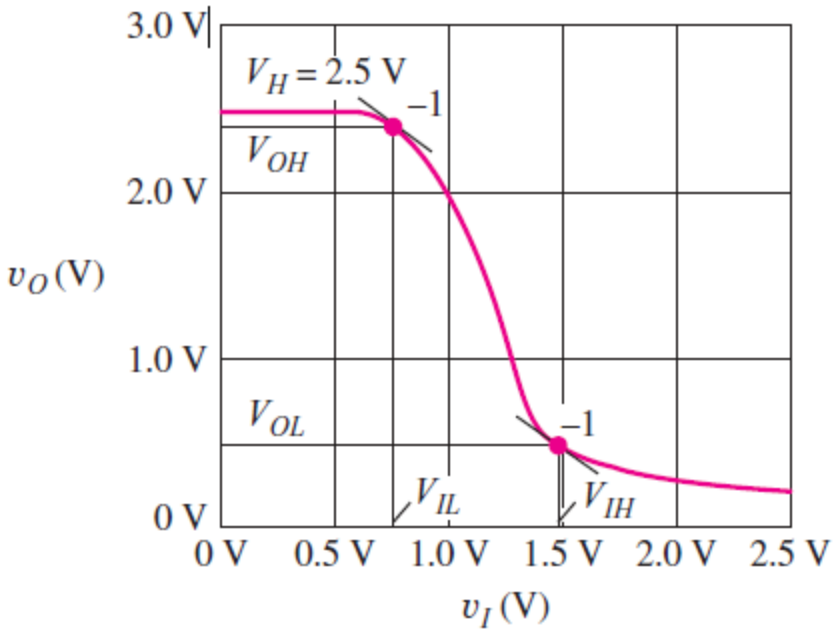
- Load Line: $v_O = V_{DD} - i_D R$ ②
- Combine ①②:

$$v_I = V_{TN} + \frac{v_O}{2} + \frac{V_{DD} - v_O}{K_n R v_O}$$

$$\Rightarrow \frac{dv_I}{dv_O} = \frac{1}{2} - \frac{V_{DD}}{K_n R v_O^2}$$

- Setting $\frac{dv_I}{dv_O} = -1$, we get
  - $V_{OL} = \sqrt{\frac{2V_{DD}}{3K_n R}} = 0.816\sqrt{\frac{V_{DD}}{K_n R}}$
  - $V_{IH} = V_{TN} - \frac{1}{K_n R} + 2\sqrt{\frac{2V_{DD}}{3K_n R}}$

Calculate noise margin



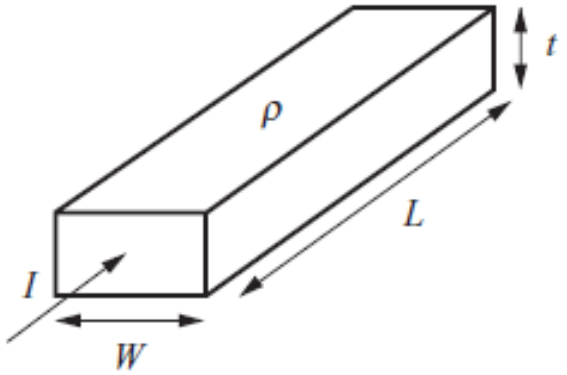
A long chain of such inverters can tolerate noise and process variations around 0.25 V in the low-input state and 0.96 V in the high state.

$$\mathrm{NM}_H = V_{DD} - V_{TN} + \frac{1}{2K_nR} - 1.63\sqrt{\frac{V_{DD}}{K_nR}}$$

$$\mathrm{NM}_L = V_{TN} + \frac{1}{K_nR} - 0.816\sqrt{\frac{V_{DD}}{K_nR}}$$

- Noise margins increase as K_nR increases for typical values of K_nR greater than 2.
- For the previous design
  - $V_{IL} = 0.756\ \mathrm{V},\ V_{OH} = 2.42\ \mathrm{V}$
  - $V_{IH} = 1.46\ \mathrm{V},\ V_{OL} = 0.51\ \mathrm{V}$
  - $\mathrm{NM}_H = 0.96\ \mathrm{V}, \mathrm{NM}_L = 0.25\ \mathrm{V}$

Load resistor



Geometry of a simple rectangular resistor

t: typically 1 µm

ρ: 10^{-3} Ω cm

- Resistance of the resistor:

$$R = \frac{\rho L}{tW}$$

- Consider a 28.8 k Ω load:

$$\frac{L}{W} = \frac{Rt}{\rho} = \frac{2.88 \times 10^4\ \Omega\ 10^{-4}\text{cm}}{0.001\ \Omega\ \text{cm}} = \frac{2880}{1}$$

- If width is 1 µm, length has to be 2.88 mm!
- Load resistor takes too much area on a chip
- Alternatives ??

